IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in the application:

1. (Currently Amended): A system, comprising:

a Central Processing Unit (CPU) coupled to an external memory and one or more peripherals; and

a Physics Processing Unit (PPU) coupled to the CPU and a Physics Processing Memory (PPM) and comprising a PPU Control Engine (PCE), a Data Movement Engine (DME), a DME control interface and a Floating Point Engine (FPE), wherein

the PCE is configured to control the overall operation of the PPU by receiving ~~receive~~ physics simulation requests from the CPU via a PPU software driver executing on the CPU, issuing ~~and to issue~~ commands to the DME and the FPE to perform physics simulation computations associated with the physics simulation requests, and allocating memory resources within the PPM to the DME and the FPE,

the DME is configured to transfer physics data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more banks of the at least one PPU internal memory,

the DME control interface is coupled to each of the PCE and the DME and comprises a first packet queue for receiving command packets from the PCE and transmitting the command packets to the DME, and a second packet queue receiving response packets from the DME and transmitting the response packets to the PCE, and

the FPE is configured to perform multiple, parallel floating point operations to generate physics simulation data associated with the physics simulation requests, wherein each parallel floating point operation is specified by a very long instruction word (VLIW) that is issued to the FPE by the PCE ~~is configured to respond to commands from at least one of the PCE and the DME and to execute floating point computations on physics data stored in the at least one PPU internal memory~~.

2. (Original): The system of claim 1, wherein the CPU comprises a processing unit resident in a personal computer.

3. (Original): The system of claim 1, wherein the CPU comprises a processing unit resident in a game console.

4. (Original): The system of claim 1, further comprising:

a Graphics Processing Unit (GPU) operatively connected to the CPU.

5. (Previously Presented): The system of claim 1, wherein the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

6. (Cancelled)

7. (Previously Presented): The system of claim 1, wherein the PCE comprises programming code stored in a memory resident within the PPU.

8. – 9. (Cancelled)

10. (Previously Presented): The system of claim 1, wherein the PPM comprises high-speed memory and the PPU further comprises a high-speed data bus connecting the high-speed memory to at least one of the DME and the FPE.

11. (Original): The system of claim 10, further comprising:

a memory interface unit managing data communication between the high-speed data bus and the high-speed memory.

12. (Original): The system of claim 10, further comprising:

a processor bus connecting the PCE with at least one physical interface to the CPU.

13. (Original): The system of claim 12, wherein the processor bus is separate from the high-speed bus and connected to the high-speed bus via a bridge.

14. (Previously Presented): The system of claim 1, further comprising:

an Inter-Engine Memory (IEM) coupled to the DME and the FPE and configured to receive physics simulation data from the PPM in response to commands received from the DME.

15. (Previously Presented): The system of claim 14, further comprising:

an Inter-Engine Register (IER) coupled to the DME and the FPE and adapted to initiate DME operation in response to a PCE command.

16. (Previously Presented): The system of claim 14, wherein the IEM comprises multiple banks of memory adapted to support parallel threads of execution.

17. (Previously Presented): The system of claim 15, wherein the IER comprises multiple banks of registers, and wherein the IEM comprises multiple banks of memory adapted to support two parallel threads of execution.

18. – 19. (Cancelled)

20. (Previously Presented): The system of claim 16, further comprising:

a Scratch Pad Memory (SPM) configured to receive data from the PPM in response to commands from the DME;

wherein the IEM further comprises a first bank accessible to the DME and a second bank accessible to the FPE; and,

wherein the DME further comprises:

a first unidirectional crossbar connected to the first bank;

a second unidirectional crossbar connected to the second bank; and,

a bi-directional crossbar connecting the first and second crossbars to at least one of the PPM or SPM.

21. (Previously Presented): The system of claim 20, wherein the DME further comprises:

a first Address Generation Unit providing Read address data to the first unidirectional crossbar; and,

a second Address Generation Unit providing Write address data to the second unidirectional crossbar.

22. (Original): The system of claim 10, wherein the FPE further comprises:
a plurality of floating point operation execution units.

23. (Original): The system of claim 22, wherein the plurality of floating point execution units are selectively grouped together to form a vector floating point unit.

24. (Cancelled)

25. (Currently Amended): A game system, comprising:

a host, wherein the host comprises an external memory and a peripheral coupled to a Central Processing Unit (CPU); and,

a Physics Processing Unit (PPU) coupled to the CPU and a Physics Processing Memory (PPM) and comprising a PPU Control Engine (PCE), a Data Movement Engine (DME), a DME control interface and a Floating Point Engine (FPE),

the PCE is configured to control the overall operation of the PPU by receiving ~~receive~~ physics simulation requests from the CPU via a PPU software driver executing on the CPU, issuing ~~and to issue~~ commands to the DME and the FPE to perform physics simulation computations associated with the physics

simulation requests, and allocating memory resources within the PPM to the DME and the FPE,

the DME is configured to transfer physics data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more banks of the at least one PPU internal memory,

the DME control interface is coupled to each of the PCE and the DME and comprises a first packet queue for receiving command packets from the PCE and transmitting the command packets to the DME, and a second packet queue receiving response packets from the DME and transmitting the response packets to the PCE, and

the FPE is configured to perform multiple, parallel floating point operations to generate physics simulation data associated with the physics simulation requests, wherein each parallel floating point operation is specified by a very long instruction word (VLIW) that is issued to the FPE by the PCE ~~is configured to respond to commands from at least one of the PCE and the DME and to execute floating point computations on physics data stored in the at least one PPU internal memory~~;

wherein the host stores a main game program and the PPU software driver; and,

wherein the PPU software driver manages all communication between the PPU and the CPU.

26. (Previously Presented): The game system of claim 25, wherein the host further stores:

a first Application Programming Interface (API) associated with the main game program; and

a second API associated with the PPU driver.

27. (Original): The game system of claim 26, wherein the second API is callable by the first API.

28. (Original): The game system of claim 27, wherein the host further comprises a Graphics Processor Unit (GPU), wherein the host further stores:

a GPU driver and a third API associated with the GPU driver;

wherein the second API is callable by the first and third APIs.

29. (Previously Presented): The game system of claim 25, wherein the PPU further comprises a dedicated vector processor adapted to perform parallel floating point operations.

30. (Original): The game system of claim 29, wherein the PPU further comprises a high-speed memory.

31. (Currently Amended): A personal computer system (PC) executing a game program on hardware comprising a memory, a peripheral, and a general purpose microprocessor, the PC further comprising:

a Physics Processing Unit (PPU) coupled to a Physics Processing Memory (PPM) and comprising a PPU Control Engine (PCE), a Data Movement Engine (DME), a DME control interface and a Floating Point Engine (FPE), wherein

the PCE is configured to control the overall operation of the PPU by receiving ~~receive~~ physics simulation requests from a Central Processing Unit (CPU) via a PPU software driver executing on the CPU, issuing ~~and issue~~ commands to the DME and the FPE to perform physics simulation computations associated with the physics simulation requests, and allocating memory resources within the PPM to the DME and the FPE,

the DME is configured to transfer physics data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more banks of the at least one PPU internal memory,

the DME control interface is coupled to each of the PCE and the DME and comprises a first packet queue for receiving command packets from the PCE and

transmitting the command packets to the DME, and a second packet queue receiving response packets from the DME and transmitting the response packets to the PCE, and

the FPE is configured to perform multiple, parallel floating point operations to generate physics simulation data associated with the physics simulation requests, wherein each parallel floating point operation is specified by a very long instruction word (VLIW) that is issued to the FPE by the PCE ~~is configured to respond to commands from at least one of the PCE and the DME and to execute floating point computations on physics data stored in the at least one PPU internal memory~~.

32. (Previously Presented): The PC of claim 31, wherein the PPU is operatively connected within the PC by means of an expansion board.

33. (Original): The PC of claim 32, further comprising a Graphics Processing Unit (GPU) adapted to compute graphics data for incorporation within execution of the game program.

34. (Original): The PC of claim 31, wherein the general purpose microprocessor generates a command in response to execution of the game program and communicates the command to the PPU.

35. (Previously Presented): The PC of claim 34, wherein the PPU and general purpose microprocessor communicate via at least one selected from a group of physical interfaces consisting of Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

36. (Original): The PC of claim 35, wherein the PPU comprises a vector processor adapted to run parallel floating point operations.

37. (Cancelled)

38. (Previously Presented): The system of claim 1, wherein the PCE is configured to call microcode routines executed within the DME and FPE to perform physics simulation computations.

39. (Previously Presented): The game system of claim 25, wherein the PCE is configured to call microcode routines executed within the DME and FPE to perform physics simulation computations.

40. (Previously Presented): The PC of claim 31, wherein the PCE is configured to call microcode routines executed within the DME and FPE to perform physics simulation computations.